CESGA en colaboración con USC, UDC y UVIGO PRESENTA la CONFERENCIA del

Dr. Roger Espasa

INGENIERO del EQUIPO DE DISEÑO Intel DE LA FAMILIA DE MICROPROCESADORES XeonPhi

"Arquitecturas para hacer frente a los retos planteados por HPC y BigData"

CICLO DE CONFERENCIAS ABIERTAS DEL MASTER EN COMPUTACIÓN DE ALTAS PRESTACIONES

Lugares: Salón de actos CITIUS, USC (Campus Vida), Santiago de Compostela (USC)
Por videoconferencia Coruña: Salón de Grados, Facultad de Informática (UDC)
Por videoconferencia Ourense: Salón de Grados, Edificio Politécnico, Campus As Lagoas, Ourense (UVIGO)

Fecha: Martes, 26 de noviembre de 2013
Hora: 16:00h.
Duración: 2 horas (1h 30' Conferencia + 30' preguntas)

Dirigido a: Investigadores, Ingenieros y Estudiantes interesados en arquitecturas de procesadores, retos que las aplicaciones HPC y BigData suponen para el hardware.

Registro: La asistencia es abierta y no requiere registro previo.

Idioma: La conferencia se impartirá en lengua Española.

Abstract: In this talk we will describe the technology trends that dictate how microprocessors need to evolve to support HPC and BigData applications. We'll discuss how these two application areas are converging. We'll cover how HPC applications need to scale to leverage large number of cores and what are the choices for the core designer to support HPC/BigData needs.

Biography: Roger Espasa got his Phd in 1997 with UPC. In 1999-2001 he worked for the Alpha Microprocessor Group on a vector extension to the Alpha architecture. The project, codenamed Tarantula, was an 8-way SMT EV8 coupled to a large vector unit. In 2002, the Alpha team, and the tiny subsidiary that had been created in Barcelona to work on Tarantula was acquired by Intel. Since then Roger has been working at Intel, where he currently is a Principal Engineer. At Intel, Roger worked first on a vector extension for Nehalem, that evolved into the AVX1 instruction set. In 2005, Roger started working on the vector instruction set for the Knights Ferry architecture that later evolved in the recently released AVX-512 instruction set. Roger is currently working on the XeonPhi family of microprocessors where he oversees the definition for its cores.

Más Información: www.cesga.es

USC UNIVERSIDADE DE SANTIAGO DE COMPOSTELA · UNIVERSIDADE DA CORUÑA · Universidade de Vigo · CESGA